Amendments to the Claims:

A listing of the entire set of pending claims (including amendments to the claims, if any) is submitted herewith per 37 CFR 1.121. This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1 (Canceled)

2. (Currently amended) ~~A data processing apparatus according to Claim 1~~ The apparatus of claim 6, wherein clock signals to the functional units and/or parts of the instruction memory in the subset are disabled in ~~said~~ the power saving state.

3. (Currently amended) ~~A data processing apparatus according to Claim 1~~ The apparatus of claim 6, wherein the functional units are organized into groups of one or more functional units each, the functional unit or units in each respective group receiving instructions from a respective instruction field in the instruction word, each time for execution by one of the functional units in the group, the power saving circuit selecting the functional units that are switched to the power saving state per group.

4. (Currently amended) ~~A data processing apparatus according to Claim 1~~ The apparatus of claim 6, wherein the instruction memory system comprises a plurality of memory units, each for supplying a respective instruction field in the instruction word for an instruction for a respective functional unit or group of functional units, the ~~clock gating~~ power saving circuit being arranged to switch those memory units to the power saving state that supply the instruction field that for the selectable ones of the functional units that are switched to the power saving state.

5. (Currently amended) ~~A data processing apparatus according to Claim 4, wherein~~ A data processing apparatus comprising:

[[-]] an instruction memory system arranged to output an instruction word, capable of containing a plurality of instructions, respective instruction words being output in response to respective instruction addresses;

[[-]] an instruction execution unit, comprising a plurality of functional units, each capable of executing a respective instruction from the instruction word in parallel with execution of other instructions from the instruction word by other ones of the functional units;

[[-]] a power saving circuit arranged to switch a selectable subset of the functional units and/or parts of the instruction memory that supply instructions from the instruction word to the functional units to a power saving state during program execution, the power saving circuit being arranged to select the functional units and/or parts of the instruction memory in the subset dependent on program execution;

wherein:

the instruction memory system includes a plurality of memory units, each for supplying a respective instruction field in the instruction word for an instruction for a respective functional unit or group of functional units, the clock gating circuit being arranged to switch those memory units to the power saving state that supply the instruction field for the selectable ones of the functional units that are switched to the power saving state, and

the memory units each comprise memory locations for at least a part of each instruction words only for instruction words in a respective range of instruction addresses, the instruction memory system allowing for partial overlap of the respective ranges of different ones of the memory units.

6. (Currently amended) ~~A data processing apparatus according to Claim 1~~ A data processing apparatus comprising:

[[-]] an instruction memory system arranged to output an instruction word, capable of containing a plurality of instructions, respective instruction words being output in response to respective instruction addresses;

[[-]] an instruction execution unit, comprising a plurality of functional units, each capable of executing a respective instruction from the instruction word in parallel with execution of other instructions from the instruction word by other ones of the functional units;

[[-]] a power saving circuit arranged to switch a selectable subset of the functional units and/or parts of the instruction memory that supply instructions from the instruction word to the functional units to a power saving state during program execution, the power saving circuit being arranged to select the functional units and/or parts of the instruction memory in the subset dependent on program execution;

wherein the power saving circuit is arranged to select the subset dependent an instruction address associated with the instruction word.

7. (Currently amended) ~~A data processing apparatus according to Claim 1~~ The apparatus of claim 6, wherein the power saving circuit is arranged to select the subset under control of one or more instructions contained in a program executed by the data processing apparatus.

8. (Currently amended) ~~A data processing apparatus according to Claim 7~~ The apparatus of claim 7, wherein ~~said~~ the one or more instructions specify the subset.

9. (Currently amended) A method of executing a program of instructions using ~~a data processing apparatus according to Claim 1~~ the apparatus of claim 6, the method comprising identifying a part of the program wherein the instruction word does not contain instructions for functional units in a particular one of the groups, and using the power saving circuit to switch to the power saving state the functional units that

not contained in the particular one of the groups and/or memory units that are coupled to the particular one of the groups, during executing ~~of said~~ the identified part of the program.

10. (New) The apparatus of claims 6, including:

a control memory that is configured to store a plurality of address ranges of the instruction addresses associated with the instruction words, and

a controller that is configured to control the power saving circuit based on a comparison of an address of a current instruction word to the address ranges.

11. (New) A data processing apparatus comprising:

an instruction memory system arranged to output an instruction word, capable of containing a plurality of instructions, respective instruction words being output in response to respective instruction addresses;

an instruction execution unit, comprising a plurality of functional units, each capable of executing a respective instruction from the instruction word in parallel with execution of other instructions from the instruction word by other ones of the functional units; and

a power saving circuit arranged to switch a selectable subset of the functional units and/or parts of the instruction memory that supply instructions from the instruction word to the functional units to a power saving state during program execution, the power saving circuit being arranged to select the functional units and/or parts of the instruction memory in the subset dependent on program execution;

wherein at least one of the functional units is configured to:

receive a power saving instruction from the instruction word, and

control the power saving circuit to switch at least one other functional unit to the power saving state based on the power saving instruction.

12. (New) The apparatus of claim 11, wherein clock signals to the functional units and/or parts of the instruction memory in the subset are disabled in the power saving state.

13. (New) The apparatus of claim 11, wherein the instruction memory system comprises a plurality of memory units, each for supplying a respective instruction field in the instruction word for an instruction for a respective functional unit or group of functional units, the clock power saving circuit being arranged to switch those memory units to the power saving state that supply the instruction field that for the selectable ones of the functional units that are switched to the power saving state.